UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/815,772	03/22/2001	Johni Chan	69907	5285

22242 7590 11/14/2003

FITCH EVEN TABIN AND FLANNERY
120 SOUTH LA SALLE STREET
SUITE 1600
CHICAGO, IL 60603-3406

EXAMINER	
MASON, DONNA K	

ART UNIT	PAPER NUMBER
2181	4

DATE MAILED: 11/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PR4

Office Action Summary	Application No.	Applicant(s)	
	09/815,772	CHAN, JOHNI	
	Examiner	Art Unit	
	Donna K. Mason	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☒ Claim(s) *6, 8-13, and 16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a)☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

On page 1, line 33, change "performs" to --perform--;

On page 6, line 12, change "year" to --rear--;

On page 7, lines 27-32, the sentence, "Because each of the single board computers . . . in the tremendous amount of functionality is available to the user of the computer system", is incomprehensible;

On page 8, line 11, change "120" to --120--;

On page 8, line 22, insert --210, 212-- after "(system host)";

On page 8, line 26, insert --210-- after "computer".

Appropriate correction is required. See 37 CFR 1.71.

Claim Objections

2. Claims 6, 8-13 and 16-18 are objected to because of the following informalities:

In claim 6, line 1, change "A apparatus" to --An apparatus--;

The examiner urges the applicant to review all the claims for use of the terms "another" and "other." To provide clarity, the examiner recommends changing "another" and/or "other" to --first--, --second--, --third--, etc., where appropriate. For example, the following changes are suggested:

In claim 6, line 2, insert --first-- before "hybrid";

In claim 6, line 6, insert --first-- before "switch";

In claim 6, line 8, insert --first-- before "bridge";

In claim 8, line 2, insert --first-- before "bridge";

In claim 9, line 2, change "another" to --a second--;

In claim 10, line 2, change "another" to --a second--;

In claim 11, line 3, insert --first-- before "bridge";

In claim 11, line 4, change "other" to --second--;

In claim 12, line 5, change "another" to --a second--;

In claim 12, line 6, change "other" to --second--;

In claim 12, line 7, change "other" to --second--;

In claim 13, line 7, insert --first-- before "hybrid";

In claim 16, line 2, change "another" to --a second--;

In claim 17, line 3, insert --first-- before "hybrid";

In claim 17, line 5, change "other" to --second--;

In claim 18, line 3, insert --first-- before "hybrid";

In claim 18, line 5, change "another" to --a second--;

In claim 18, line 6, change "other" to --second--; and

In claim 18, line 7, change "other" to --second--.

Appropriate correction is required. See 37 CFR 1.71.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,574,950 to Hathorn, et al. ("Hathorn").

With regard to independent claim 1, and as shown in Fig. 3, Hathorn discloses a system (item 300), including a first processor (item 301) including a first processor data channel (item 302), a first hybrid switching module (item 305) including a first hybrid switching module processor data channel (item 341), a first hybrid switching module main data channel (item 349), a first input/output link data channel (item 351), and a first switch (item 305), the first hybrid switching module processor data channel being coupled to the first processor data channel. Hathorn also discloses a first main bus (item 324) coupled to the first hybrid switching module main data channel (item 349), a second processor (item 311) including a second processor data channel (item 312), and a second hybrid switching module (item 315). The second hybrid switching module includes a second hybrid switching module processor data channel (item 344), a

second input/output link data channel (item 351), and a second switch (item 315), the second hybrid switching module processor data channel being coupled to the second processor data channel, and the second input/output link data channel being coupled to the first input/output link data channel.

With regard to dependent claim 2, Hathorn discloses the system where the second hybrid switching module further includes a second hybrid switching module main data channel (item 345), where the system further includes a second main bus (item 334) coupled to the second hybrid switching module main data channel.

Therefore, Hathorn reads on the invention as claimed.

5. Claims 1-13 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,643,795 to Fu, et al. ("Fu").

With regard to independent claim 1, and as shown in Fig. 12, Fu discloses a system, including a first processor (CPU0) including a first processor data channel (see MP CPU bus between CUP0 and FCU-MCU 0), a first hybrid switching module (FCU-MCU 0) including a first hybrid switching module processor data channel (see MP CPU bus between CUP0 and FCU-MCU 0), a first hybrid switching module main data channel (see PT-TO-PT channel between FCU-MCU 0 and I/O bridge chip), a first input/output link data channel (see PT-TO-PT channel between FCU-MCU 0 and FCU-MCU 1), and a first switch (see column 2, lines 65-67), the first hybrid switching module processor data channel being coupled to the first processor data channel. Fu also discloses a first main bus (see PT-TO-PT channel between FCU-MCU 0 and I/O bridge

chip) coupled to the first hybrid switching module main data channel, a second processor (CPU4) including a second processor data channel (see MP CPU bus between CUP4 and FCU-MCU 1), and a second hybrid switching module (FCU-MCU 1). The second hybrid switching module includes a second hybrid switching module processor data channel (see MP CPU bus between CUP4 and FCU-MCU 1), a second input/output link data channel (see PT-TO-PT channel between FCU-MCU 0 and FCU-MCU 1), and a second switch (see column 2, lines 65-67), the second hybrid switching module processor data channel being coupled to the second processor data channel, and the second input/output link data channel being coupled to the first input/output link data channel.

With regard to dependent claim 2, Fu discloses the system where the second hybrid switching module further includes a second hybrid switching module main data channel (see PT-TO-PT channel between FCU-MCU 1 and I/O bridge chip), where the system further includes a second main bus (see PT-TO-PT channel between FCU-MCU 1 and I/O bridge chip) coupled to the second hybrid switching module main data channel.

With regard to dependent claim 3, Fu discloses a third processor (CPU8) including a third processor data channel (see MP CPU bus between CPU8 and FCU-MCU 2), and a third hybrid switching module (FCU-MCU 2) including a third hybrid switching module processor data channel (see MP CPU bus between CPU8 and FCU-MCU 2), a third input/output link data channel (see PT-TO-PT channel between FCU-MCU 0 and FCU-MCU2), a fourth input/output link data channel (see PT-TO-PT

channel between FCU-MCU 1 and FCU-MCU 2), and a third switch (see column 2, lines 65-67), the third hybrid switching module processor data channel being coupled to the third processor data channel. Fu also discloses the system where the first hybrid switching module further includes a fifth input/output link data channel (see PT-TO-PT channel between FCU-MCU 0 and FCU-MCU 2), where the third input output link data channel is coupled to the fifth input/output link data channel, where the second hybrid switching module further includes a sixth input/output link data channel (see PT-TO-PT channel between FCU-MCU 1 and FCU-MCU 2), and where the fourth input/output link data channel is coupled to the sixth input/output link data channel.

With regard to dependent claim 4, Fu discloses the system where the second hybrid switching module further includes a second hybrid switching module main data channel (see PT-TO-PT channel between FCU-MCU 1 and I/O bridge chip), where the system further includes a second main bus (see PT-TO-PT channel between FCU-MCU 1 and I/O bridge chip) coupled to the second hybrid switching module main data channel.

With regard to dependent claim 5, Fu discloses the system where the third hybrid switching module further includes a third switching module main data channel (see PT-TO-PT channel between FCU-MCU 2 and I/O bridge chip), where the system further includes a third main bus (see PT-TO-PT channel between FCU-MCU 2 and I/O bridge chip) coupled to the second hybrid switching module main data channel.

With regard to independent claim 6, Fu discloses an apparatus including a (first) hybrid switching module processor data channel (see MP CPU bus between CPU0 and

FCU-MCU 0), a hybrid switching module main data channel (see PT-TO-PT channel between FCU-MCU 0 and I/O bridge chip), an input/output link data channel (see PT-TO-PT channel between FCU-MCU 0 and FCU-MCU 1), a (first) switch (see column 2, lines 65-67) coupled to the hybrid switching module processor data channel, and a (first) bridge (see I/O bridge chip connected to FCU-MCU 0) coupled to the hybrid switching module data channel. As disclosed, the switch selectively couples to the bridge and selectively couples to the input/output link data channel, where the hybrid switching module processor data channel is thereby selectively coupled to the bridge and selectively coupled to the input/output link data channel.

With regard to dependent claims 7-10, Fu further discloses a processor (CPU0) couple to the hybrid switching module processor data channel, a main bus (see PT-TO-PT channel between FCU-MCU 0 and I/O bridge chip) coupled to the (first) bridge, a (second) switch (FCU-MCU 1) coupled to the input/output link data channel, and a (second) bridge (see I/O bridge chip connected to FCU-MCU 1) coupled to the (second) switch.

With regard to dependent claim 11, Fu further discloses a first main bus (see PT-TO-PT channel between FCU-MCU 0 and I/O bridge chip) coupled to the (first) bridge, and a second main bus (see PT-TO-PT channel between FCU-MCU 1 and I/O bridge chip) coupled to the (second) bridge.

With regard to dependent claim 12, Fu further discloses a first processor (CPU0) coupled to the hybrid switching module processor data channel, and a second processor (CPU4) coupled to a (second) hybrid switching module processor data

channel (see MP CPU bus between CPU4 and FCU-MCU 1), the (second) switch being coupled to the second hybrid switching module processor data channel.

With regard to independent claim 13, Fu discloses a system including a hybrid switching module processor data channel (see MP CPU bus between CPU0 and FCU-MCU 0), a hybrid switching module main data channel (see PT-TO-PT channel between FCU-MCU 0 and I/O bridge chip), a hybrid switching module bus data channel (see connection between I/O bridge chip and PCI bus), an input/output link data channel (see PT-TO-PT channel between FCU-MCU 0 and FCU-MCU 1), and a (first) hybrid switching module (FCU-MCU 0) coupled to the hybrid switching module processor data channel and to the hybrid switching module main data channel, where the hybrid switching module selectively couples to the hybrid switching module bus data channel and selectively couples to the input/output link data channel, and where the hybrid switching module processor data channel is thereby selectively coupled to the hybrid switching module bus data channel and selectively coupled to the input/output link data channel.

With regard to dependent claims 14-16, Fu further discloses a processor (CPU0) coupled to the hybrid switching module processor data channel, a main bus (PCI bus) coupled to the hybrid switching module bus data channel, and a (second) hybrid switching module (FCU-MCU 1) coupled to the input/output link data channel.

With regard to dependent claim 17, Fu further discloses a first main bus (see PCI bus) coupled to the (first) hybrid switching module, and a second main bus (see PCI bus) coupled to the (second) hybrid switching module.

With regard to dependent claim 18, Fu further discloses a first processor (CPU0) coupled to the (first) hybrid switching module processor data channel, and a second processor (CPU1) coupled to a (second) hybrid switching module processor data channel, the (second) hybrid switching module being coupled to the (second) hybrid switching module processor data channel.

Therefore, Fu reads on the invention as claimed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna K. Mason whose telephone number is (703) 305-1887. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (703) 305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

XUAN M. THAI
PRIMARY EXAMINER
TC2100

DKM